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CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY

Applicant: Jeffrey S. Mailloux et al.

Serial No.: 08/984,562

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Paragraph 1, on page 1:

FI
This application is a divisional of application Serial No. 08/650,719, filed May 20, 1996, which is a Continuation-In-Part of application Serial No. 08/584,600, filed January 1, 1996, now U.S. Patent No. 5,966,724.

Paragraph beginning on page 38, line 11:

LI
In column-based switching, switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles. Moreover, this type of switching may be accomplished on either read or write cycles, *e.g.*, from a burst EDO read cycle to a pipelined EDO read cycle and vice-versa, or from a burst EDO write cycle to a pipelined EDO write cycle and vice-versa.